

Atty Docket No.: CPH35726-D

Serial No.: 10/072,362

**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Claims 1-9 (canceled)**

10. (Currently Amended) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thick insulating layer disposed over said first and second trench, the thick insulating layer partially filling said first and second trench profile and being conformal to said first and second trench profile;

a gate electrode disposed over said thick insulating layer in said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion ~~being~~ is embedded inside the first trench completely filling a remaining portion of the first trench, the second vertical portion ~~being~~ is embedded inside the second trench completely filling a remaining portion of the second trench, and the horizontal portion ~~being~~ is disposed over the substrate and ~~connecting~~ connects said first and second vertical portions together; and

a first shallow doped region within the substrate disposed at an upper corner adjacent to

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the first vertical portion and a second shallow doped region disposed at an upper corner adjacent to the second vertical portion of the electrode; and

a first deep source region extending from the first shallow doped region and a second deep drain region extending from the second shallow doped region are disposed in a region within the substrate deeper than the first and second trenches.

11. (Previously Added) The structure according to claim 10, wherein the thick insulating layer is formed by thermal oxidation.

12. (Previously Added) The structure according to claim 10, wherein the thickness of the thick insulating layer is about 0.1  $\mu\text{m}$ .

13. (Currently Amended) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

a thick insulating layer disposed over said first and second trench, the thick insulating layer being conformal to said first and second trench profile;

a gate electrode disposed over said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion ~~being~~ is embedded inside the first trench, the second vertical portion ~~being~~ is

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embedded inside the second trench, and the horizontal portion ~~being~~ is disposed over the substrate and ~~connecting~~ connects said first and second vertical portions together; and

a first shallow doped region having dopants of first type within the substrate disposed at an upper corner adjacent to the first vertical portion and a second shallow doped region having dopants of first type disposed at an upper corner adjacent to the second vertical portion of the electrode; and

a first deep source region having dopants of second type extending from the first shallow doped region and a second deep drain region having dopants of second type extending from the second shallow doped region are disposed in a region within the substrate deeper than the first and second trenches.

14. (Previously Added) The structure according to claim 13, wherein the thick insulating layer is formed by thermal oxidation.

15. (Previously Added) The structure according to claim 13, wherein the thickness of the thick insulating layer is about 0.1  $\mu\text{m}$ .

16. (Currently Amended) A semiconductor structure comprising a substrate having an active region of a first conductive type including a channel region and a non-channel region surrounding the channel region, at least a first trench and a second trench disposed in the active region, the structure comprising:

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~~a thick insulating layer disposed over said first and second trench, the thick insulating layer being conformal to said first and second trench profile;~~

a gate electrode disposed over said first and second trenches, the gate electrode comprising a first vertical portion, a second vertical portion and a horizontal portion, wherein the first vertical portion ~~being~~ is embedded inside the first trench, the second vertical portion ~~being~~ is embedded inside the second trench, and the horizontal portion ~~being~~ is disposed over the substrate and ~~bisecting~~ connects said first and second vertical portions together; and

a first shallow doped region having a dopant of first conductive type within the substrate disposed at an upper corner adjacent to the first vertical portion and a second shallow doped region having a dopant of first conductive type disposed at an upper corner adjacent to the second vertical portion of the electrode; and

a first deep source region having a dopant of second conductive type extending from the first shallow doped region and a second deep drain region having a dopant of second conductive type extending from the second shallow doped region are disposed in a region within the substrate deeper than the first and second trenches.

17. (Previously Added) The structure according to claim 16, wherein the thick insulating layer is formed by thermal oxidation.

18. (Previously Added) The structure according to claim 16, wherein the thickness of the thick insulating layer is about 0.1  $\mu\text{m}$ .

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**AMENDMENTS TO THE DRAWINGS**

The attached sheets of drawings include changes to Fig.2C and Fig. 4D. These sheets, which include Fig. 2A-2C, and Fig. 4C-4D replaces the original sheets including Fig.2A-2C and Fig. 4C-4D. In Figure 2C, previously having informal hand writing has been removed, and in Fig. 4D, a boundary is shown between the shallow doped region 304 and the deep doped region 306.

Attachment: Replacement Sheet

Annotated Sheet Showing Changes